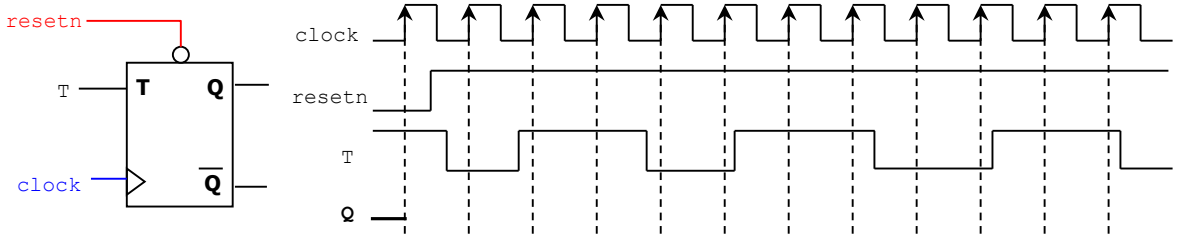
Homework 3

(Due date: March 10th @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

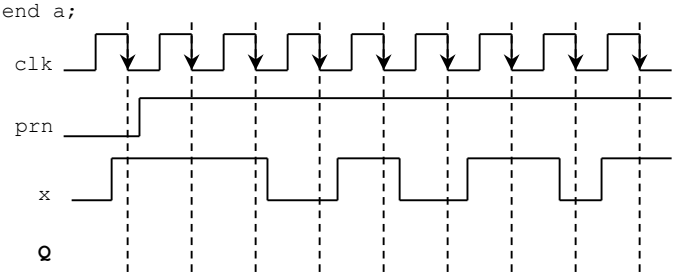
PROBLEM 1 (25 PTS)

a) Complete the timing diagram of the circuit shown below. (5 pts)

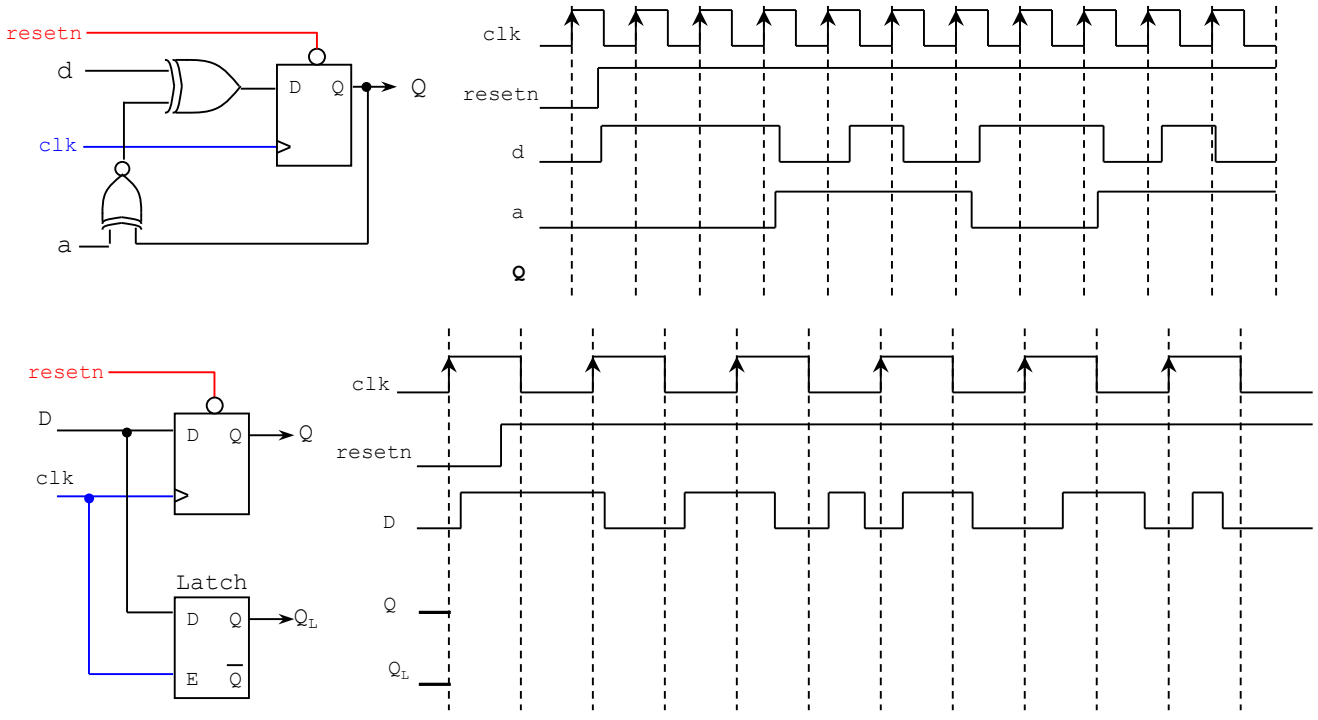


b) Complete the timing diagram of the circuit whose VHDL description is shown below: (5 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( prn, x, clk: in std_logic;
         q: out std_logic);
end circ;

architecture a of circ is

   signal qt: std_logic;

begin
   process (prn, clk, x)
   begin
     if prn = '0' then
        qt <= '1';
     elsif (clk'event and clk = '0') then
        if x = '1' then
           qt <= not(qt);
        end if;
     end if;
   end process;
   q <= qt;
end a;
```

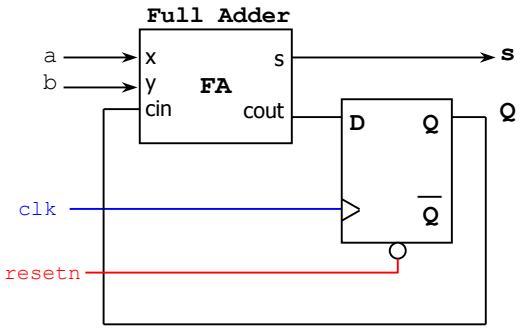


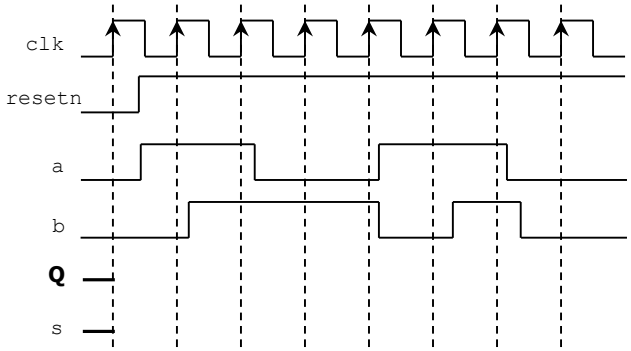
c) Complete the timing diagram of the circuits shown below: (15 pts)



PROBLEM 2 (15 PTS)

- Complete the timing diagram of the circuit shown below: (8 pts)





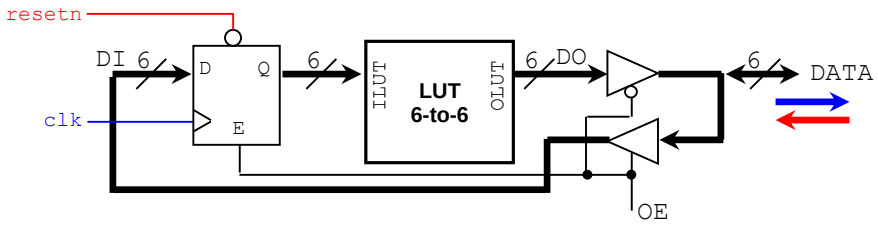
- Complete the VHDL description of the synchronous sequential circuit whose truth table is shown below: (7 pts)

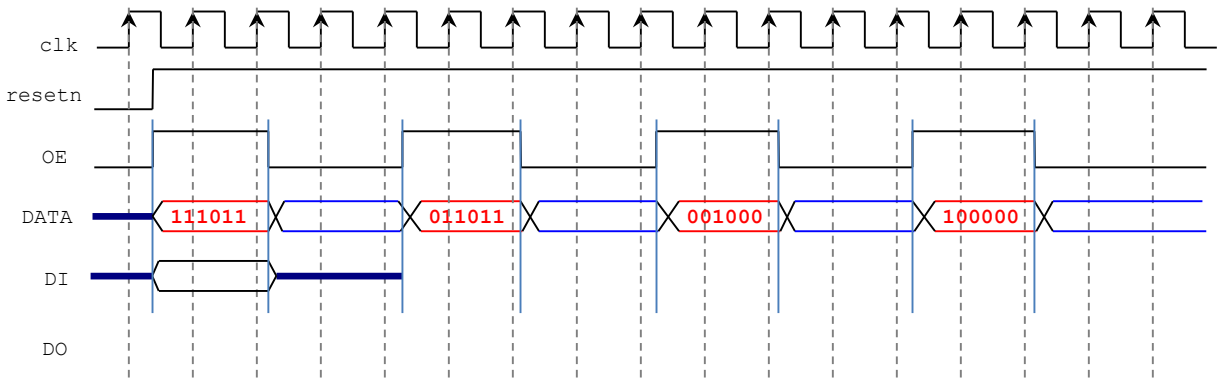
```
library ieee;
use ieee.std_logic_1164.all;

entity my_ff is
  port ( a, b, c: in std_logic;
         prn, clk: in std_logic;
         q: out std_logic);
end my_ff;

architecture a of my_ff is

begin
   -- ???
end a;
```

prn	clk	A	B	Q_{t+1}
1	↑	0	0	$\overline{Q_t}$
1	↑	0	1	Q_t
1	↑	1	0	B
1	↑	1	1	$\overline{C}$
0	X	X	X	1

PROBLEM 3 (20 PTS)

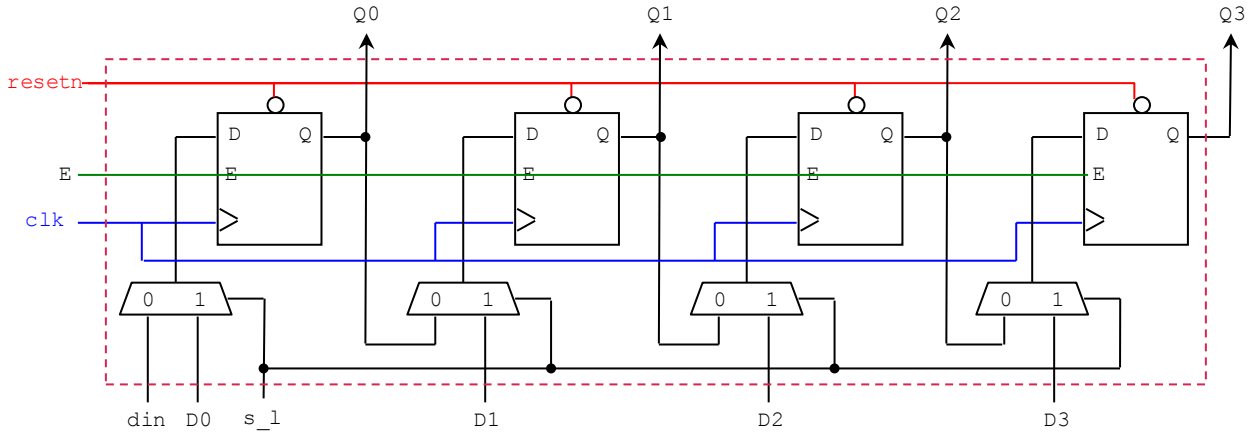
- Given the following circuit, complete the timing diagram (signals DO and $DATA$).
  The LUT 6-to-6 implements the following function: $OLUT = \lceil ILUT^{0.95} \rceil$.
  For example $ILUT = 35\ (100011_2) \rightarrow OLUT = \lceil 35^{0.95} \rceil = 30\ (011110_2)$

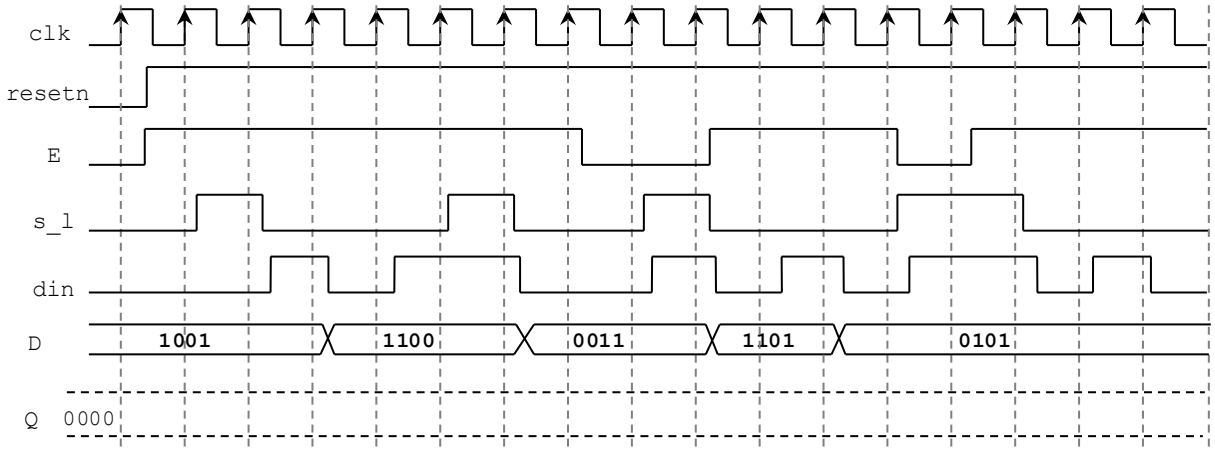




PROBLEM 4 (30 PTS)

- The following circuit is a 4-bit parallel/serial load shift register with enable input.
  Shifting operation: `s_l=0`. Parallel load: `s_l=1`. Note that $Q = Q_3Q_2Q_1Q_0$. $D = D_3D_2D_1D_0$
  - ✓ Write a structural VHDL code. You MUST create a file for: i) flip flop, ii) MUX 2-to-1, and iii) top file (where you will interconnect the flip flops and MUXes). Provide a printout. (10 pts)
  - ✓ Write a VHDL testbench according to the timing diagram shown below. Complete the timing diagram by simulating your circuit (Timing Simulation). The clock frequency must be 50 MHz with 50% duty cycle. Provide a printout. (20 pts)





PROBLEM 5 (10 PTS)

- Attach a printout of your Initial Project Report (no more than a page). This report should contain the project title, the project description, and the current status of the project. Use the provided template (`Final Project – Report Template.docx`).